

What is claimed is:

1       1. An electronic package comprising:

2           a first circuitized substrate having at least one conductive aperture therein having an  
3           external surface;

4           a second circuitized substrate having at least one conductive aperture therein having an  
5           external surface, said first and second circuitized substrates aligned such that said at least one  
6           conductive aperture of said first circuitized substrate is substantially aligned with said at least one  
7           conductive aperture of said second circuitized substrate; and

8           at least one solder member including a first contact portion extending from said external  
9           surface of said conductive aperture of said first circuitized substrate and a second contact portion  
10          extending substantially within both of said aligned conductive apertures of said first and second  
11          circuitized substrates to secure said circuitized substrates together.

1       2. The electronic package of claim 1 wherein said first and said second circuitized substrates  
2          are comprised of a material selected from the group consisting of polyimide,  
3          polytetrafluoroethylene and epoxy glass cloth.

1       3. The electronic package of claim 2 wherein said first and second circuitized substrates are  
2          flexible.

1       4. The electronic package of claim 1 wherein said at least one conductive aperture of said  
2          first circuitized substrate and said at least one conductive aperture of said second circuitized  
3          substrate comprises a hole having a cylindrical shape.

1       5.     The electronic package of claim 1 wherein said at least one conductive aperture of said  
2 first circuitized substrate and said at least one conductive aperture of said second circuitized  
3 substrate include a conductive layer thereon.

1       6.     The electronic package of claim 5 wherein said conductive layers of said apertures are  
2 comprised of metallic material.

1       7.     The electronic package of claim 6 wherein said metallic material is selected from the  
2 group consisting of copper, nickel, gold, chromium, solder and alloys thereof.

1       8.     The electronic package of claim 7 wherein said metallic material includes a protective  
2 layer thereon, said protective layer selected from the group consisting of benzatriazole, chlorite,  
3 or immersion tin.

1       9.     The electronic package of claim 1 where said solder member is comprised of a high melt  
2 solder alloy having a melting point temperature greater than about 183 degrees Celsius..

1       10.    The electronic package of claim 9 wherein said high melt solder alloy is comprised of  
2 metallic material, said metallic material is selected from the group consisting of tin, lead, gold,  
3 silver, antimony, and combinations thereof.

1       11.    The electronic package of claim 1 wherein said first contact portion of said solder  
2 member extending from said external surface of said conductive aperture of said first circuitized  
3 substrate includes a cross-sectional configuration that is substantially round, oval, or ellipsoidal.

1       12.    The electronic package of claim 11 wherein said first contact portion of said solder  
2 member extending from said external surface of said conductive aperture of said first circuitized  
3 substrate forms a connection to a printed circuit board.

- 1       13. The electronic package of claim 1 wherein said second contact portion of said solder  
2 member extends at least to said external surface of said conductive aperture of said second  
3 circuitized substrate.
- 1       14. The electronic package of claim 13 wherein said second contact portion of said solder  
2 member is substantially in the form of a dome on said external surface of said conductive  
3 aperture of said second circuitized substrate.
- 1       15. The electronic package of claim 13 wherein said second contact portion of said solder  
2 member is at least one of an array of solder members on said external surface of said conductive  
3 aperture of said second circuitized substrate.
- 1       16. The electronic package of claim 15 further including at least one integrated circuit chip,  
2 said chip being attached to said array of said solder members.
- 1       17. The invention of claim 1 wherein said electronic package is a single chip carrier.
- 1       18. The invention of claim 1 wherein said electronic package is a multi-chip module  
2 including at least two chips.
- 1       19. A method of making an electronic package comprising the steps of:  
2              providing a first circuitized substrate having at least one conductive aperture therein  
3              having an external surface;  
4              providing a second circuitized substrate having at least one conductive aperture therein  
5              having an external surface;  
6              aligning said first and second circuitized substrates such that said at least one conductive

7       aperture of said first circuitized substrate is substantially aligned with said at least one conductive  
8       aperture of said second circuitized substrate; and

9                  forming at least one solder member including a first contact portion extending from said  
10         external surface of said conductive aperture of said first circuitized substrate and a second  
11         contact portion extending substantially within both of said aligned conductive apertures of said  
12         first and second circuitized substrates, said solder member securing said circuitized substrates  
13         together.

1       20.      The method of claim 19 wherein said step of providing said conductive apertures in said  
2       first and second circuitized substrates further comprises the steps of providing first and second  
3       dielectric layers and drilling, punching or ablating at least one aperture in each of said dielectric  
4       layers.

1       21.      The method of claim 20 wherein said step of providing said conductive apertures in said  
2       first and second circuitized substrates further comprises the step of plating, sputtering or  
3       evaporating said at least one aperture in each of said dielectric layers.

1       22.      The method of claim 21 wherein said step of providing said conductive apertures in said  
2       first and second circuitized substrates further comprises the step of metallizing said apertures  
3       with copper, nickel, gold, chromium, solder, or alloys thereof.

1       23.      The method of claim 19, wherein said forming said at least one solder member comprises  
2       the steps of :

3                  providing at least one solder portion on said external surface of said conductive aperture  
4       of said first circuitized substrate and in substantial contact with said conductive aperture of said  
5       first circuitized substrate;

6                  contacting said external surface of said conductive aperture of said second circuitized

7       substrate with a heated member;

8               applying a specified force to said external surface of said conductive aperture of said  
9       second circuitized substrate; and

10              applying an energy pulse to said heated member in contact with said external surface of  
11       said conductive aperture of said second circuitized substrate to melt said at least one solder  
12       portion forming said solder member.

1       24.   The method of claim 23 wherein said step of forming said at least one solder member  
2       further comprises extending said second contact portion at least to said external surface of said  
3       conductive aperture of said second circuitized substrate.

1       25.   The method of claim 24 wherein said extending said second contact portion at least to  
2       said external surface of said conductive aperture of said second circuitized substrate further  
3       comprises the step of forming said second contact portion into substantially the shape of a dome  
4       on said external surface of said conductive aperture of said second circuitized substrate.